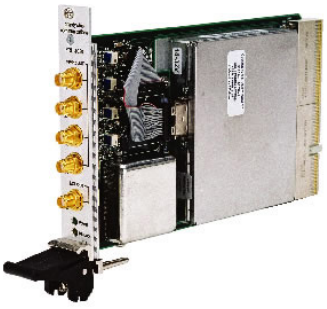
TIME & FREQUENCY SOLUTIONS
BY BRANDYWINE COMMUNICATIONS

CPCI-SyncClock32
Bus-Level Timing Board

The CPCI-SyncClock32 Bus-Level Timing Board provides precision time with zero latency to the host computer over the CPCI bus.



Features

- 32 bit 6U CPCI module
- IRIG A, B, NASA 36, 1 PPS sync inputs
- GPS sync option (maintains single-slot)
- Have Quick sync input option
- Propagation delay correction
- Zero latency time reads
- Match Time output
- IRIG-B time code output (Option)
- External Event time tags
- Three user programmable rates

Key Benefits

An on-board microprocessor automatically synchronizes the clock to reference signal inputs. The reference signal inputs can be 1 PPS, IRIG or NASA time codes and optionally, GPS or Have Quick. The clock can free run and be set by commands from the host over the CPCI bus.

The on-board clock accepts an IRIG A, B, or NASA 36 input and accepts user input reference input signal delay information. An IRIG B code generator is also included.

The advanced microprocessor on the PCI-SyncClock32 module constantly measures the time error between the on-board clock and the reference input code and adjusts the error measurement for propagation delay. In units with a disciplined TCXO or OCXO the residual error is used in an adaptive gain loop to adjust the frequency of the oscillator for minimum error. If the incoming time code is missing, or corrupted by noise, the on-board clock is updated using the disciplined 10 MHz oscillator. When the input code is again useable the correction loop is smoothly closed.

BCD time data is available to the host computer using two zero latency time reads. The time message contains units of microseconds through units of years. A status word is available using an additional read.

The time-of-occurrence of random external events may be captured (time-tagged) by using the Event Time input. When the event input is sensed the current time is saved in a buffer for later interrogation by the host. The resolution of the time tag is 100 nanoseconds.

Internal or external processes may be automatically initiated or terminated by using the Match Time feature. This feature asserts an output when the clock's time matches that of the user input start time. The output is terminated under user control or when the pre-programmed stop time is encountered. The resolution of the Match Time comparison is one microsecond.

Three user programmable pulse rates are provided. Two pulse rates, Clock Low and Clock High, are available on the multi-pin connector. The third rate generator provides heartbeat timing to the host. The divider for each of the three rate generators is programmable by the host over the range 2–65,535. The inputs to the rate generators are 3 MHz or 100 Hz for the heartbeat, 3 MHz for Clock High and 100 Hz for Clock Low.

The GPS synchronization option adds worldwide time transfer capability that can be traced to the U.S. Government standard UTC-USNO. Very precise synchronization, automatic leap year and leap second correction, and accurate position information are additional benefits provided by the GPS option.

Software packages for Windows 95/98, Windows NT, DOS and VxWorks are available. C language samples are supplied with the CPCI-SyncClock32.

In addition to the comprehensive set of standard capabilities of the CPCI-SyncClock32, we offer a wide range of options that may be specified. These options allow the user to customize the CPCI-SyncClock32 to fit almost any application.

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CPCI-SyncClock32 Specifications

General Input Specifications

Input Codes	IRIG A & B, NASA 36 (1kHz Carrier)
Input Amplitude	.25 to 10 Vpp
Input Impedance	>10k Ohms
Ratio	2:1 to 6:1
Frequency Error	100 PPM maximum
Code Sync Accuracy	One microsecond
1PPS Input	TTL, positive edge
1PPS Sync Accuracy	One microsecond
External Event	TTL, positive or negative edge
Resolution	100 nanoseconds–units of year
Min. event spacing	None

General Output Specifications

IRIG B DC Shift	TTL (Option)
Match Pulse	TTL level at Start-Stop time
Resolution	Microseconds-eight milliseconds
Clock Low Rate	TTL, negative going
Clock Divisor	2–65,535
Clock Input	100 PPS
Default output	1 PPS
Clock High Rate	TTL, negative going
Clock Divisor	2–65,535
Clock Input	3 MPPS
Default output	76.923k PPS
Heartbeat Rate	Interrupt, flag, TTL and negative going
Clock Divisor	2–65,535
Clock Input	100 PPS or 3 MPPS
Default output	1k PPS
BCD Time	Microseconds–unit year on demand, zero latency 58 bits in two 32 bit words
Status word	8 bits
Status LED	Flashes coded patterns
Interrupts	External Event, RAM FIFO, Heartbeat, Match Time
Flags	Dual Port RAM data ready, FIFO data ready, In sync, Heartbeat, Match Time, External Event
Connectors	BNC, high density DB-26

Mechanical & Environmental

Size	6U
Type	Single-slot 32-bit 5V CPCI
Power	
+5Vdc	±5%, 400 mA maximum
+12 Vdc	±5%, 100 mA maximum
-12Vdc	±5%, 50 mA maximum
Operating Temperature	0°C to +70°C
Storage Temperature	-40°C to +85°C
Humidity	To 95% without condensation

Options

GPS Sync Input	C/A code
Sync Accuracy	100 nanoseconds
Position Accuracy	25 meters SEP
Tracking	Eight parallel channels
Antenna	L1 magnetic mount, 25' cable
Antenna Options	
Hi-gain	L1, mast mount, 100' cable
Fiber Optic Kit	Fiber optic transmitter-receiver pair for long antenna cable runs
Differential GPS Inputs	Per RTCM 104
IRIG B Modulated Output	2.5 Vpp into 600 Ohms
Input Code Isolation	Transformer coupling
Input Codes	IRIG G, XR3, 2137, IRIG E, 109-60
Output codes	IRIG A, NASA 36, IRIG G
Eight External Event Inputs	TTL positive or negative edge
Have Quick Input	Per ICD–GPS–060
Have Quick Output	Per ICD–GPS–060
Binary Time Words	Replaces BCD
Oscillator Upgrades	Disciplined TCXO, 1 PPM Disciplined OCXO, .01 PPM
1 PPS 10 Vdc input	Sync input, +10 Vdc, 50 ohms
STANAG 4430	Time code sync input
STANAG 4430	Time code output
IRIG B D.C. shift time code	TTL
Software packages	Windows NT, 2000 Windows 95/98, Linux

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